REMARKS

Claims 1-65 are pending in the present application. Claims 1, 54, 57, 60 and 65 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Claims 54-56 and 65 stand rejected under 35 U.S.C. 102(e) as being anticipated by Gillingham, *et al.* (U.S. Patent No. 6,510,503). Claims 1-4, 6-9, 11 and 60-61 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth (U.S. Patent No. 6,029,250). Claim 5 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth, and further in view of Gasbarro, *et al.* (U.S. Patent No. 5,432,823). Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Moyal, *et al.* (U.S. Patent No. 6,326,853). Claim 12 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Wada, *et al.* (U.S. Patent No. 6,029,250). Claims 13-15 and 22-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Yoshitake (U.S. Patent No. 6,043,704). Claim 57 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Chan, *et al.* (U.S. Patent No. 5,998,860). Reconsideration and removal of the rejections and allowance the claims are respectfully requested.

With regard to the rejection of claims 1 and 60, in the present invention as claimed in independent claim 1, a memory system having a stub configuration includes "a controller for generating a first clock signal". A memory module receives the first clock signal from the controller and, in response to a read command, generates "a second clock signal in response to the first clock signal", and the "data signals and the second clock signal" are "output from the memory module in synchronization with the first clock signal". The "second clock signal" is "provided to the controller" and the "controller" receives "the data signals on the data bus in

response to the second clock signal during the read operation".

In the present invention as claimed in independent claim 60, a method of transferring data in a memory system having a stub configuration includes "generating a first clock signal...at a controller". The method further includes generating a "second clock signal" at a memory module "in response to the first clock signal" and "outputting the data signals and the second clock signal in synchronization with the first clock signal". The "second clock signal" is "provided to the controller" and the "controller" receives "the data signals on the data bus in response to the second clock signal during the read operation".

Gillingham, *et al.* is cited in the Office Action as disclosing a memory system having a stub configuration (see Gillingham column 10, lines 10-57 and column 11, lines 23-59). A controller 82 generates a free running reference clock CLK. Source synchronous data clocks dclk0 and dclk1 are provided by the controller 82 for timing data in a source synchronous manner. During a read operation, memory devices 84 drive one of the data clocks dclk0 and dclk1 in a source synchronous manner along with read data on the data bus, and the controller 82 schedules which of the data clocks to use, such that the controller 82 knows which data clock to use to latch in read data. Separate programmable fine vernier delays 107 and 108 receive as inputs the clock signal CLK and delay the rising and falling edges to generate delayed even and odd signals OUTCLKE and OUTCLKO which drive the clock input of respective D-type latches 120 and 122 for latching even and odd output data signals. Data clocks dclk0 and dclk1 are delayed by programmable delays 109 and 110 to produce separate even and odd delayed clocks.

It is stated in the Office Action with regard to independent claims 1 and 60 that Gillingham, *et al.* does not discuss that details of clock generations in the memory module. Thus, Gillingham, *et al.* fails to teach or suggest a memory system that includes a "memory module" in which "data signals" and a "second clock signal" are "output from the memory module in synchronization with" a received "first clock signal", as claimed in claim 1. In addition, Gillingham, *et al.* fails to teach or suggest a method of transferring data in a memory

system that includes a memory module outputting "data signals" and a "second clock signal in synchronization with" a received "first clock signal", as claimed in claim 60.

Keeth discloses a read synchronization system 400 including a read FIFO buffer 420 that generates differential data clock signals DCLK0 and DCLK1 in response to a read clock signal RCLK (see Keeth, FIG. 4). Data words RSDW<0:15> are clocked into the read FIFO buffer 420 in response to the RCLK signal, and are clocked out of the read FIFO buffer 420 in response to a DRCLK signal having a phase difference relative to the RCLK signal that is determined by a current value of a phase command word CMDPH<0:3>. The read synchronization data words RSDW <0:15> are thus clocked out of the read FIFO buffer 420 having a timing offset relative to the data clock signals DCLK0 and DCLK1. Thus the data output to the memory controller 402 are not in synchronization with DCLK0 and DCLK1. The memory controller 402 latches the data words in response to the differential clock signals DCLK0, DCLK1. In addition, in Keeth, the RCLK signal is apparently derived from a clock generator 40 that generates a number of clock signals to be used on the memory module, in response to a received command clock CCLK (see FIG. 3 of Keeth and the corresponding discussion at column 3, lines 48-53).

Keeth fails to teach or suggest a memory system that includes a "memory module" in which "data signals" and a "second clock signal" are "output from the memory module in synchronization with" a "first clock signal", as claimed in claim 1. Instead, in Keeth, the read synchronization data words RSDW <0:15> are clocked out of the read FIFO buffer 420 using the DRCLK signal having a timing offset relative to the data clock signals DCLK0 and DCLK1. In addition, there is no teaching or suggestion in Keeth that the Keeth RCLK signal is generated "in synchronization with" the received Keeth CCLK signal, as claimed in claim 1. Further, Keeth fails to teach or suggest a method of transferring data in a memory system that includes a memory module outputting "data signals" and a "second clock signal in synchronization with" a "first clock signal", as claimed in claim 60 for similar reasons.

Neither Gillingham, *et al.* nor Keeth teaches or suggests a memory system that includes a

"memory module" in which "data signals" and a "second clock signal" are "output from the memory module in synchronization with" a "first clock signal", as claimed in claim 1. Further, neither Gillingham, *et al.* nor Keeth teaches or suggests that a method of transferring data in a memory system includes a memory module outputting "data signals" and a "second clock signal in synchronization with" a "first clock signal", as claimed in claim 60. Accordingly, it is submitted that the combination of Gillingham, *et al.* nor Keeth fails to teach or suggest the invention as claimed in claims 1 and 60. Reconsideration of the rejection of, and allowance of, claims 1 and 60 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* and Keeth are respectfully requested. With regard to the dependent claims 3-4, 6-9, 11 and 61, it follows that these claims should inherit the allowability of the independent claims from which they depend.

With regard to the rejection of claim 5 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.*, Keeth, and Gasbarro, *et al.*, Gasbarro, *et al.* is cited in the Office Action as disclosing a system wherein the propagation delay of a clock signal from a device to a master is substantially equal to that of a data bus. Like Gillingham, *et al.* and Keeth, Gasbarro, *et al.* fails to teach or suggest a memory system that includes a "memory module" in which "data signals" and a "second clock signal" are "output from the memory module in synchronization with" a "first clock signal", as claimed. Accordingly, it is submitted that the combination of Gillingham, *et al.*, Keeth and Gasbarro, *et al.* fails to teach or suggest the invention as claimed. Reconsideration of the rejection of, and allowance of, claim 5 are respectfully requested.

With regard to the rejection of claim 10 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.*, Keeth, and Moyal, *et al.*, Moyal, *et al.* is cited in the Office Action as disclosing a system comprising a capacitor having a capacitance that is selected to compensate for capacitive loading. Like Gillingham, *et al.* and Keeth, Moyal, *et al.* fails to teach or suggest a memory system that includes a "memory module" in which "data signals" and a "second clock signal" are "output from the memory module in synchronization with" a "first clock signal", as claimed. Accordingly, it is submitted that the combination of Gillingham, *et al.*, Keeth and

Moyal, *et al.* fails to teach or suggest the invention as claimed. Reconsideration of the rejection of, and allowance of, claim 10 are respectfully requested.

With regard to the rejection of claim 12 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.*, Keeth, and Wada, *et al.*, Wada, *et al.* is cited in the Office Action as disclosing a memory system wherein first and second signal lines are crossed between first and second modules. Like Gillingham, *et al.* and Keeth, Wada, *et al.* fails to teach or suggest a memory system that includes a "memory module" in which "data signals" and a "second clock signal" are "output from the memory module in synchronization with" a "first clock signal", as claimed. Accordingly, it is submitted that the combination of Gillingham, *et al.*, Keeth and Wada, *et al.* fails to teach or suggest the invention as claimed. Reconsideration of the rejection of, and allowance of, claim 12 are respectfully requested.

With regard to the rejection of claims 13-15 and 22-24 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.*, Keeth, and Yoshitake, Yoshitake is cited in the Office Action as disclosing a system wherein a return clock signal line is coupled to a dummy load. Like Gillingham, *et al.* and Keeth, Yoshitake fails to teach or suggest a memory system that includes a "memory module" in which "data signals" and a "second clock signal" are "output from the memory module in synchronization with" a "first clock signal", as claimed. Accordingly, it is submitted that the combination of Gillingham, *et al.*, Keeth and Yoshitake fails to teach or suggest the invention as claimed. Reconsideration of the rejection of, and allowance of, claims 13-15 and 22-24 are respectfully requested.

With regard to the rejection of independent claims 54 and 65, in the present invention as claimed in independent claim 54, a memory system having a stub configuration includes "a controller for generating a first clock signal" and a "second clock signal generator independent of the controller for generating a second clock signal". A "memory module including memory devices coupled to the controller" receives "the first clock signal" and "the second clock signal".

In the present invention as claimed in independent claim 65, a method of transferring data in a memory system having a stub configuration includes "generating a first clock signal...at a controller", and "generating a second clock at a second clock signal generator independent of the controller". The method further includes "receiving the first clock signal" and "the second clock signal...at a memory module".

Gillingham, et al. fails to teach or suggest a memory system that includes "a controller for generating a first clock signal" and a "second clock signal generator independent of the controller for generating a second clock signal", as claimed in claim 54. Instead, in Gillingham, et al., the controller 82 generates the free running reference clock CLK, and OUTCLKE and OUTCLKO are delayed even and odd signals of the clock signal CLK, thus the programmable fine vernier delays 107 and 108 are not generating a new signal. Similarly, the programmable delays 109 and 110 produce separate even and odd delayed clocks of the dclk0 and dclk1 clocks, they do not generate a new clock signal. Further, the data clocks dclk0 and dclk1 are provided by the controller 82 for timing data in a source synchronous manner, and during a read operation, memory devices 84 drive one of the data clocks dclk0 and dclk1 in a source synchronous manner along with read data on the databus, the controller 82 scheduling which of the data clocks should be used, such that the controller knows which data clock to use to latch in read data. Therefore, Gillingham, et al. does not disclose a "second clock signal generator independent of" a "controller" as claimed in claim 54. Further, Gillingham, et al. fails to teach or suggest a method of transferring data in a memory system that includes "generating a second clock at a second clock signal generator independent" of a "controller", as claimed in claim 65. Instead, in Gillingham, et al., the controller 82 generates the free running reference clock CLK, and during a read operation, memory devices 84 drive one of the data clocks dclk0 and dclk1 in a source synchronous manner along with read data on the databus and the controller 82 schedules which of the data clocks should be used, such that the controller knows which data clock to use to latch in read data. Reconsideration and removal of the rejection of claims 54 and 65 under 35 U.S.C. 102(e) as being anticipated by Gillingham, et al. are therefore respectfully requested. With regard to the dependent claims 55 and 56, it follows that these claims should inherit the

allowability of the independent claims from which they depend.

With regard to the rejection of independent claim 57, under 35 U.S.C. 103(a) as being unpatentable over the combination of Gillingham, *et al.*, Keeth and Chan, *et al.*, in the present invention as claimed in independent claim 57, a memory system having a stub configuration includes "a controller for generating a first clock signal". A "memory module having first and second faces" generates "a second clock signal in response to the first clock". "Data signals and the second clock signal" are "output from the memory module in synchronization with the first clock signal". The "second clock signal" is "provided to the controller" and the "controller" receives "the data signals on the data bus in response to the second clock signal during the read operation".

As stated above, Gillingham, *et al.* fails to teach or suggest a memory system that includes a "memory module having first and second faces" that outputs "data signals" and a "second clock signal" which are "in synchronization with the first clock signal", as claimed in claim 57.

Also, as stated above, Keeth fails to teach or suggest a memory system that includes a "memory module having first and second faces" that outputs "data signals" and a "second clock signal" which are "in synchronization with the first clock signal", as claimed in claim 57.

Chan, *et al.* discloses a double-sided inline memory module 20 (see Chan, *et al.*, FIG. 1). Like Gillingham, *et al.* and Keeth, Chan, *et al.* fails to teach or suggest a memory system that includes a "memory module having first and second faces" that outputs "data signals" and a "second clock signal" which are "in synchronization with the first clock signal", as claimed in claim 57. Accordingly, it is submitted that the combination of Gillingham, *et al.*, Keeth and Chan, *et al.* fails to teach or suggest the invention as claimed. Reconsideration of the rejection of, and allowance of, claim 57 are respectfully requested.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

Date: October 25, 2005

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900, Ext. 4902
Facsimile: (617) 742-7774
J:\SAM\0204\amenda\amendmenta2.wpd

Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant